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09/960,728	09/24/2001	Dominic Hugo Symes	550-258	4210

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,728	SYMES, DOMINIC HUGO	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 10/26/2005.

Information Disclosure Statement

3. The information disclosure statement filed on May 24, 2005, fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of foreign documents 10-512069 and 10-512070, which are not in the English language. It has been placed in the application file, but the information referred to therein has not been considered. See MPEP 609.04(a).

4. MPEP 609.05(a) states "If an item of information in an IDS fails to comply with all the requirements of 37 CFR 1.97 and 37 CFR 1.98, that item of information in the IDS will not be considered and a line should be drawn through the citation to show that it has not been considered." It should be noted that items are only initialed if they are considered. Consequently, the items have not been initialed.

Claim Objections

5. Claim 1 is objected to because of the following informalities: In line 4, insert a dash between "multiple" and "data". Appropriate correction is required.

6. Claim 15 is objected to because of the following informalities: In line 4, replace "operaiton" with --operation--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-9 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 5-88887 (as disclosed by applicant, applied in the previous Office Action, and herein referred to as JP) in view of Chan et al., U.S. Patent No. 5,276,881 (as applied in the previous Office Action and herein referred to as Chan).

9. Referring to claim 1, JP has taught apparatus for processing data, said apparatus comprising:

(i) a shifting circuit. See Fig.4 and page 8, lines 6-7, and note that data in shift register SR1 is shifted (inherently by a shifting circuit in response to an instruction).

(ii) a bit portion selecting and combining circuit. Again, from Fig.4 it can be seen that a 6-bit portion from SR1 is selected and combined with a 10-bit portion selected from SR2.

(iii) an instruction decoder responsive to a single-instruction-multiple-data instruction to control said shifting circuit and said bit portion selecting and combining circuit for performing an operation upon a data word Rn and a data word Rm (it is inherent that an instruction decoder exists in order to decode instructions prior to execution. The decoder, in response to the RML instruction (see page 7, lines 22-28, and page 8, line 27), will control the system such that the disclosed operation of Fig.4 is performed. In addition, the RML instruction is a single instruction with multiple data operands, where the multiple operands are the shift amount k, a first register (whose contents are stored in SR1), and either a second register or a memory address (whose contents are stored in SR2) (see Fig.4 and page 7, lines 9-13)), wherein said operation yields a value given by:

(a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See Fig.4 and note that a 10-bit portion from SR2 (Rn) is selected. Note that the 10-bit potion extend from the left end of SR2 (the 10 most significant bits). Also, it should be realized that an alternate interpretation would include selecting a 6-bit portion from the right end SR2.

(b1) selecting a second portion of bit length B of said data word Rm subject to a right shift specified as a shift operand within said single-instruction-multiple-data instruction. See Fig.4 and note that SR1 (Rm) is shifted right 10 bits and a 6-bit portion of SR1 is selected. It should be noted that the shift amount is specified by the instruction. See page 7, lines 9-17, and lines 22-26, and note that in the example given , the shift amount is 10.

(b2) JP has not explicitly taught the type of right shift that occurs with respect to Rm. (i.e., it has not been explicitly taught that the right shift is an arithmetic right shift). However,

Chan has taught that a shift can either be of the arithmetic type (where, as is known in the art, a sign bit is shifted in) or of the logical type (where, as is known in the art, a zero is shifted in). See column 29, lines 20-23. Where signed numbers are used, an arithmetic shift may be performed (so that negative numbers may have the appropriate sign bit shifted in). It should be noted from Fig.4 of JP, that it does not matter which type of shift is performed because the selected data from SR1 does not include any shifted-in data. For instance, note that in step (1), SR1 is shifted right 10 bits, and the result is shown in step (3) where the shifted-in data is shown as being blank because it is irrelevant. The only relevant portion of SR1 in step (3) is the lower 6-bit portion. Nevertheless, an arithmetic shift is useful for systems which implement a signed binary numbering system, which in turn allows for the representation of negative numbers. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP to have the right shift be an arithmetic right shift because the type of right shift is irrelevant in JP and it is also useful in shifting negative numbers.

(c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. See Fig.4 and page 8, lines 7-12, and note that the 6-bit portion from Rm and the 10-bit portion from Rn are concatenated and stored in temporary register TR0 (Rd).

10. Referring to claim 2, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said first portion extends from a most significant bit end of said data word Rn. See Fig.4, step (2), and note that the 10-bit portion extends from the most significant bit end of SR2 (Rn).

11. Referring to claim 3, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said first portion extends from a least significant bit end of said data word Rn. See Fig.4, step (2), and note that the taking the alternate interpretation of claim 1, when the first portion is the 6-bit portion of SR2, the portion extends from the least significant end, as can be seen. This 6-bit portion is still combined with the shifted data from SR1. See page 8, lines 7-9, and note that the SR registers are linked (i.e., all data within them are "combined") and then shifted.

12. Referring to claim 4, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said shift operand can specify a number of bit-positions representing an amount of arithmetic right shift to apply to said data word Rm. See page 7, lines 9-11 and note that the instruction specifies a shift amount of "k" bits (in the example given, k=10).

13. Referring to claim 5, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said first portion and said second portion abut within said output data word Rd. See Fig.4, step (4) and note that the 6-bit portion from Rm and the 10-bit portion from Rn are concatenated (they abut) in the output.

14. Referring to claim 6, JP in view of Chan has taught an apparatus as described in claim 5. JP has further taught that said output data word has a bit length of C and C = A+B. See Fig.4, step (4) and note that the output to be stored in TR0 comprises 16 bits, where 16 = 10+6.

15. Referring to claim 7, JP in view of Chan has taught an apparatus as described in claim 6. Although JP has not given a specific example showing that A=B, a person of ordinary skill in the art would've recognized that if the instruction were to specify a shift amount of 8 bits, then the A-bit portion and the B-bit portion would be 8 bits.

16. Referring to claim 8, JP in view of Chan has taught an apparatus as described in claim 1. JP in view of Chan has not taught that A = 16. However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are not given patentable weight or would have been obvious improvements. Since JP implements 16-bit registers, A cannot equal 16. However, if the JP included larger registers, which were more common in the art at the time of the invention, then more data could be stored in a register, and consequently, more values may be represented, thereby giving the system more flexibility. For instance, if a register were just one bit, then only two values could be represented (0 and 1). However, if a register were two bits, then four values could be represented (0, 1, 2, and 3). And clearly, the more data in a register, the more it could be shifted. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to increase the register size in JP and have A=16. It should be noted that JP's invention would still apply to larger registers.

17. Referring to claim 9, JP in view of Chan has taught an apparatus as described in claim 1. JP in view of Chan has not taught that B = 16. However, as shown in In re Rose, 105 USPQ 237 (CCPA 1955), changes in size/range are not given patentable weight or would have been obvious improvements. Since JP implements 16-bit registers, B cannot equal 16. However, if the JP included larger registers, which were more common in the art at the time of the invention, then more data could be stored in a register, and consequently, more values may be represented, thereby giving the system more flexibility. For instance, if a register were just one bit, then only two values could be represented (0 and 1). However, if a register were two bits, then four values could be represented (0, 1, 2, and 3). And clearly, the more data in a register, the more it could be shifted. As a result, it would have been obvious to one of ordinary skill in the art at the time

of the invention to increase the register size in JP and have B=16. It should be noted that JP's invention would still apply to larger registers.

18. Referring to claim 11, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said instruction combines a data value pack operation with a shift operation. See Fig.4, and note that data in SR1 is shifted and then data from SR1 and SR2 are packed together in a single output TR0 (step (4).

19. Referring to claim 12, JP in view of Chan has taught an apparatus as described in claim 1. JP has further taught that said shifting circuit is upstream of said selecting and combining circuit in a data path of said apparatus. Looking at Fig.4, it can be seen that the shifting (step (1)) occurs before the selecting and combination (steps (2)-(4)). Therefore, the shifting circuit is upstream of the selecting and combining circuit.

20. Referring to claim 13, JP in view of Chan has taught an apparatus as described in claim 12. JP has further taught, in what appears to be two separate ways, that said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path. First, from page 8, lines 14-25, it is disclosed that the arithmetic unit calculates a sum at some point between the data being shifted, selected, combined, and transferred to R0. Consequently, the arithmetic unit operates in parallel with the aforementioned components. Furthermore, looking at Fig.2, the arithmetic unit 9 is disposed/arranged in parallel with (next to) the SR1 and SR2 units, which may be considered part of the selecting and combining circuit since data from those units is selected and combined.

21. Referring to claim 14, JP has taught a method of data processing, said method comprising the steps of decoding and executing a single-instruction-multiple-data instruction (note that the

RML instruction is a single instruction with multiple data operands, where the multiple operands are the shift amount k, a first register (whose contents are stored in SR1), and either a second register or a memory address (whose contents are stored in SR2) (see Fig.4 and page 7, lines 9-13)) by performing an operation on a data word Rn and a data word Rm, wherein said operation yields a value given by:

a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See Fig.4 and note that a 10-bit portion from SR2 (Rn) is selected. Note that the 10-bit potion extend from the left end of SR2 (the 10 most significant bits).

b1) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said single-instruction-multiple-data instruction. See Fig.4 and note that SR1 (Rm) is shifted right 10 bits and a 6-bit portion of SR1 is selected. It should be noted that the shift amount is specified by the instruction. See page 7, lines 9-17, and lines 22-26, and note that in the example given , the shift amount is 10.

b2) JP has not explicitly taught the type of right shift that occurs with respect to Rm. (i.e., it has not been explicitly taught that the right shift is an arithmetic right shift). However, Chan has taught that a shift can either be of the arithmetic type (where, as is known in the art, a sign bit is shifted in) or of the logical type (where, as is known in the art, a zero is shifted in). See column 29, lines 20-23. Where signed numbers are used, an arithmetic shift may be performed (so that negative numbers may have the appropriate sign bit shifted in). It should be noted from Fig.4 of JP, that it does not matter which type of shift is performed because the selected data from SR1 does not include any shifted-in data. For instance, note that in step (1), SR1 is shifted right 10 bits, and the result is shown in step (3) where the shifted-in data is shown as being blank because

it is irrelevant. The only relevant portion of SR1 in step (3) is the lower 6 bits. Nevertheless, an arithmetic shift is useful for systems which implement a signed binary numbering system, which in turn allows for the representation of negative numbers. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP to have the right shift be an arithmetic right shift because the type of right shift is irrelevant in JP and it is also useful in shifting negative numbers.

c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. See Fig.4 and page 8, lines 7-12, and note that the 6-bit portion from Rm and the 10-bit portion from Rn are concatenated and stored in temporary register TR0 (Rd).

22. Referring to claim 15, JP has taught a computer program provided on a computer-readable medium, said computer program for controlling a computer to perform the steps of decoding and executing n single-instruction-multiple-data instruction (note that the RML instruction is a single instruction with multiple data operands, where the multiple operands are the shift amount k, a first register (whose contents are stored in SR1), and either a second register or a memory address (whose contents are stored in SR2) (see Fig.4 and page 7, lines 9-13)) for performing an operation upon a data word Rn and a data word Rm, wherein the operation yields a value given by:

a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See Fig.4 and note that a 10-bit portion from SR2 (Rn) is selected. Note that the 10-bit potion extend from the left end of SR2 (the 10 most significant bits).

b) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said single-instruction-multiple-data instruction. See Fig.4 and note that SR1 (Rm) is shifted right 10 bits and a 6-bit portion of SR1 is selected. It should be noted that the shift amount is specified by the instruction. See page 7, lines 9-17, and lines 22-26, and note that in the example given , the shift amount is 10.

b2) JP has not explicitly taught the type of right shift that occurs with respect to Rm. (i.e., it has not been explicitly taught that the right shift is an arithmetic right shift). However, Chan has taught that a shift can either be of the arithmetic type (where, as is known in the art, a sign bit is shifted in) or of the logical type (where, as is known in the art, a zero is shifted in). See column 29, lines 20-23. Where signed numbers are used, an arithmetic shift may be performed (so that negative numbers may have the appropriate sign bit shifted in). It should be noted from Fig.4 of JP, that it does not matter which type of shift is performed because the selected data from SR1 does not include any shifted-in data. For instance, note that in step (1), SR1 is shifted right 10 bits, and the result is shown in step (3) where the shifted-in data is shown as being blank because it is irrelevant. The only relevant portion of SR1 in step (3) is the lower 6 bits. Nevertheless, an arithmetic shift is useful for systems which implement a signed binary numbering system, which in turn allows for the representation of negative numbers. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify JP to have the right shift be an arithmetic right shift because the type of right shift is irrelevant in JP and it is also useful in shifting negative numbers.

c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. See Fig.4 and page 8, lines 7-12, and note that the 6-bit

portion from Rm and the 10-bit portion from Rn are concatenated and stored in temporary register TR0 (Rd).

It should be noted that the instruction described by Fig.4 would inherently be found in a computer program on a computer-readable medium.

Response to Arguments

23. Applicant's arguments filed on October 26, 2005, have been fully considered but they are not persuasive.

24. Applicant argues the novelty/rejection of claim 1 on pages 8-9 of the remarks, in substance that:

> "The Examiner does not identify any portion of Chan which contains such teaching and indeed the words single-instruction-multiple-data instruction or the SIMD instruction are simply missing from that reference. Moreover, there is no indication in the JP reference which suggests that such would be understood by those of ordinary skill in the art. Should the Examiner be of the opinion that there is any discussion of an SIMD instruction contained in the JP reference, he is respectfully requested to specifically point out how or why he believes this to be disclosed."

> "Because the data words in the shift registers SR1 and SR2 are linked to each other, they clearly cannot be an SIMD instruction and this fact would be clearly obvious to those even having nominal skill in the pertinent art."

25. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, it should be noted that Chan is not relied upon to show a SIMD instruction, and therefore, Chan does not have to provide such a teaching. It is the examiner's contention that JP has taught such an instruction, as claimed. More specifically, page 7, lines 9-13, of JP, state that an RML instruction includes operands including a shift amount (k), a first general register, and either a second general register or a specific memory address. The examiner asserts that this information alone is enough to anticipate the claim. The claim calls for a single-instruction-multiple-data instruction. The RML instruction is a single instruction with

multiple data operands (shift amount, first register, and either second register or memory address). Consequently, the instruction is a single-instruction-multiple-data instruction. The claim states nothing about each register, specified by the instruction, comprising multiple operands for the instruction to operate on.

b) Regarding the second argument, it is not clear how the linking of SR1 and SR2 precludes the instruction from being a single-instruction-multiple-data instruction. As the examiner previously stated, page 7, lines 9-13, of JP, have taught that the single instruction (RML) includes multiple data operands including a shift amount (k), a first general register, and either a second general register or a specific memory address. SR1 and SR2 are merely locations where data specified by the instruction is stored.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
December 20, 2005

RICHARD L. ELLIS
PRIMARY EXAMINER